WHAT IS CLAIMED IS:

1. A method for removing defects from a semiconductor surface, comprising:
coating the semiconductor surface and the defects with a protective layer;
thinning the protective layer to selectively reveal portions of the defects;
removing the defects; and
removing the protective layer.

2. The method of claim 1 wherein the coating layer provides a planar coating surface, uniformly covering the defects.

3. The method of claim 1 wherein the protective layer is a photoresist layer.

4. The method of claim 3 wherein the photoresist layer has a thickness from about 5 to about 10 microns.

5. The method of claim 4 wherein the photoresist layer has a thickness of about 8 microns.

6. The method of claim 1 wherein the protective layer is selected from a group comprising silicon oxide and silicon nitride.

7. The method of claim 6 wherein the protective layer has a thickness from about 1000 to about 6000 Angstrom.

8. The method of claim 6 wherein the protective layer is deposited using plasma enhanced chemical vapor deposition (PECVD).

9. The method of claim 3, wherein said thinning is performed using an inductively coupled plasma (ICP) oxygen process.

10. The method of claim 9, wherein the process has an etch rate of about 3000 Angstrom/minute.

11. The method of claim 3, wherein thinning is performed by reactive ion etching (RIE).

12. The method of claim 3, wherein thinning is performed by electron cyclotron resonance (ECR).

13. The method of claim 6, wherein thinning is performed by chemical-mechanical polishing (CMP).

14. The method of claim 13, wherein a KOH-based slurry is used.

15. The method of claim 6, wherein thinning is performed by means of a hydrofluoric acid (HF) solution.

16. The method of claim 15, wherein the thinning rate is of about 100 Angstrom/minute.

17. The method of claim 6, wherein thinning is performed by buffered oxide etching (BOE).

18. The method of claim 1, wherein removing of the defects is performed by etching.

19. The method of claim 1, wherein thinning the protective layer is performed by a process which is identical to a process for removing the protective layer.

20. The method of claim 1, wherein the semiconductor surface comprises a semiconductor selected from a group comprising GaSb, InAs, Si, InP, GaAs, InAs, and AlSb.

21. The method of claim 1, wherein the defects are removed using a wet chemical etchant.

22. The method of claim 21, wherein the defects are removed using a chemical etchant selected from the group comprising citric acid, HCl, and acetic acid.

23. The method of claim 21, wherein the defects are removed using a chemical etchant selected from the group comprising: i) a KOH (potassium hydroxide), water, isopropyl alcohol additive solution; ii) an ethylene diamine pyrocathecol, water, pyrazine additive solution; iii) a TMAH (tetramethyl ammonium hydroxide), water solution; and iv) a hydrazine (N_2H_4), water, isopropyl alcohol solution.

24. A method for removing defective structures from an epitaxial layer, comprising:

applying a coating layer to a surface of the epitaxial layer, the coating layer coating the surface and the defective structures;

thinning the coating layer to reveal portions of the defective structures without revealing portions of the surface of the epitaxial layer;

removing the defective structures; and

removing the coating layer.

25. The method of claim 24, wherein the epitaxial layer comprises device layers.

26. The method of claim 25, wherein the device layers are located over an etch stop layer and a substrate.

27. The method of claim 24, wherein the coating layer is a photoresist layer.

28. The method of claim 27, wherein thinning is performed through an inductively coupled plasma (ICP) process.

29. The method of claim 28, wherein the ICP process has an etch rate of about 3000 Angstrom/minute.

30. The method of claim 24, wherein the protective layer is selected from a group comprising silicon oxide and silicon nitride.

31. The method of claim 24, wherein the epitaxial layer is located over a first selective etch layer, a second selective etch layer, and a substrate.

32. The method of claim 31, wherein a spacer or protection layer is located between the first selective etch layer and the second selective etch layer.